

Europäisches Patentamt

European Patent Office

Office européen des brevets



EP 0 929 094 A2

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:

14.07.1999 Bulletin 1999/28

(21) Application number: 98310258.3

(22) Date of filing: 15.12.1998

(51) Int. Cl.6: H01L 21/00

(11)

(84) Designated Contracting States:

AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

Designated Extension States:

AL LT LV MK RO SI

(30) Priority: 07.01.1998 US 4074

(71) Applicants:

 International Business Machines Corporation Armonk, N.Y. 10504 (US)

 SIEMENS AKTIENGESELLSCHAFT 80333 München (DE) (72) Inventors:

- Muller, Paul K.
 Wappingers Falls, New York 12590 (US)
- Jaiprakash, Venkatachalam C. Beacon, New York 12508 (US)
- (74) Representative:

Davies, Simon Robert IBM, United Kingdom Limited, Intellectual Property Law,

Intellectual Property Law, Hursley Park

Winchester, Hampshire SO21 2JN (GB)

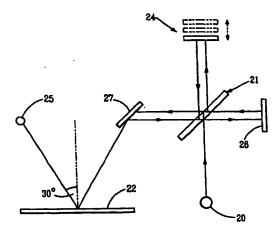
(54) Method and device for measuring the depth of a buried interface

(57) The invention discloses a method for measuring the depth at which a buried interface below the surface in a semiconductor substrate is located in a non-destructive manner which employs Fourier Transform Infrared (FTIR) measurements.

The method includes illuminating the semiconductor substrate containing the buried interface to be measured with infrared light and detecting and analyzing the spectral content of a return signal by Fourier analysis. It further involves comparing the spectral content of the return signal to calibration spectra to thereby determine the depth of the buried interface.

In addition a device is also provided for measuring the depth of a buried interface.

FIG. 5



FP 0 929 094 A

Description

[0001] The present invention is concerned with a nondestructive method for measuring the depth of a buried interface below the surface in a semiconductor substrate.

1

[0002]High processing speed in currently available data processors must be supported by large amounts of high speed random access memory. Due to reduced device counts per memory cell, much of the required storage is provided by dynamic random access memories (DRAMs) so that a significantly greater number of memory cells can be provided on a single integrated circuit chip. In such devices, the density of memory cells. principally comprising one storage capacitor per memory cell, is of great importance. The capacitance of each capacitor is very limited due to small size, while that capacitance must be large compared to the capacitance of the word line and bit line to achieve adequate operating margins for the sense amplifiers used to detect the presence or absence of stored charge. Therefore, the trenches are formed to relatively large depths while being very closely spaced. These same geometries are also important for other trench structures such as isolation trenches.

[0003] In recent years, it has also been the practice to provide a buried plate within the semiconductor substrate in which the trench capacitors are formed. The buried plate is a region surrounding the sides and bottom of a storage node trench in the dynamic random access memory cell which acts as the fixed potential terminal for the storage capacitor. The buried plate typically goes down the sides of the storage node trench about 6 microns. The depth at which the top surface of the buried plate is located should be a set distance such as 1.5 ± 0.15 microns below the surface of the semiconductor substrate. This depth of the buried plate is typically referred to as D_{BP}

[0004] The buried plate can be fabricated using resist recess processing along with outdiffusing of a dopant such as arsenic from the lower portion of a trench. U.S. Patent 5,618,751 to Golden et al and assigned to International Business Machines Corporation describes one such process. The resist recess depth and the buried plate depth are critical parameters for the trench capacitor.

[0005] Currently, measuring the buried plate depth as well as that for other buried interface structures can only be carried out destructively by cross-section and microscopic imaging of random samples.

[0006] Accordingly the invention provides a nondestructive method for measuring the depth of the top of a buried interface below the surface in a semiconductor substrate comprising:

illuminating the semiconductor substrate containing the buried interface to be measured with infrared light; detecting and analyzing the spectral content of a return signal by Fourier analysis; and comparing the spectral content of said return signal to calibration spectra to thereby determine the depth of said buried interface.

[0007] A preferred embodiment of the present invention provides a non-destructive method for measuring the depth at which the top surface of a buried interface is located in a semiconductor substrate. The buried interface depth can be determined without destructively cross-sectioning. The method of the preferred embodiment employs a Fourier Transform Infrared measure-(FTIR). This comprises subjecting semiconductor substrate containing the buried interface to a beam of infrared light and then detecting and analyzing the spectrum of a return signal by a Fourier analysis. The spectrum as analyzed by the Fourier analysis is then compared to calibration spectra to thereby determine the depth of the top surface of the buried interface. [0008] The preferred embodiment is also concerned. with a device for determining the depth of a buried interface below the surface of a semiconductor substrate. The device comprises a FTIR spectrophotometer which illuminates the substrate with a source of infrared radiation and which produces a Fourier transform of a return signal reflected from the substrate. The device also includes a library of stored calibration spectra, along with means for comparing the Fourier transform return signal to the calibration spectra to determine the depth of the buried interface.

[0009] A non-destructive method thus employs Fourier Transform Infrared (FTIR) measurements to detect the depth of a buried interface below the surface in a semiconductor substrate; i.e. to measure the depth at which the top surface of the buried interface is located. In addition a device is provided for measuring the depth of a buried interface.

[0010] A preferred embodiment of the invention will now be described in detail by way of example only with reference to the following drawings:

Figs. 1-4 are schematic diagrams illustrating a prior art process for providing a buried interface.

Fig. 5 is a schematic diagram of the arrangement employed to carry out the FTIR measurements in a preferred embodiment of the present invention.

Fig. 6 provides curves showing the spectral content of known and unknown samples having different buried plate depth measurements.

Fig. 7 is a graph that confirms the measurements obtained by the preferred embodiment compared to SEM cross-sectioning.

[0011] Referring now to the drawings, and more particularly Figs. 1-4, a typical procedure for providing a buried interface, and especially a buried conductive plate is illustrated for purposes of background. For purposes of simplicity, the following discussion is directed

Q

to a buried conductive plate as the buried interface, it being understood, of course, that the same general approach is applicable for measuring the depth of other buried interface structures marking the line between regions of significantly different dopants or between regions of significantly different doping concentrations. An example of one such buried interface in addition to a buried conductive plate is a subsurface doped region of silicon which forms a source/drain terminal or gate terminal of a vertical FET transistor within a trench. In memory arrays which have such vertical transistors, the present invention could be used to determine the depth

of such buried doped regions.

[0012] Fig. 1 illustrates a semiconductor substrate 1 such as silicon containing a trench 2. Numeral 3 represents a thin silicon nitride pad covered by a relatively thick layer 4 of tetraethylorthosilicate (TEOS). Numeral 5 represents a layer of arsenic doped silicate glass (ASG) deposited within trench 2. A photoresist 6 is provided above and within trench 2. The photoresist can be a positive photoresist such as those based upon novolak resins. As illustrated in Fig. 2, the photoresist 6 is recessed to about 1.5 microns below the substrate surface by exposure and development or dry etching. The layer 5 (ASG) is etched back in accordance with the resist recess 6 such as using a buffered hydrofluoric acid (BHF). The layer 5 is typically etched slightly below the resist recess (see Fig. 3). The remaining resist fill 6 in the trenches is then removed and then impurity diffusion or drive-in from the ASG into the substrate 1 or pwell therein is then carried out to substantially form the buried plate 7 in accordance with the location of the remaining ASG. Typical times and temperatures for the drive-in are 3 hours at 1050°C or 1 hour at 1100°C.

[0013] Samples with different D_{BP} were prepared and exposed to an infrared beam of a FTIR system. A typical FTIR system is available from Bio-Rad Laboratories under the trade designation Bio-Rad QS500. Fig. 5 illustrates a schematic of the FTIR set up. In particular, a FTIR system is an instrument which emits a controlled infrared spectrum and detects and analyzes the spectral content of a return signal by Fourier analysis. As illustrated in Fig. 5, an IR source 20 is provided such as a Globar IR source to emit broadband infrared energy for instance at wave numbers between 400 and 4500 (a wavelength range of about 25 microns to about 2 microns). An interferometer such as a Michaelson interferometer is located in the path from the IR source 20 to sample 22. The interferometer includes moving mirror 24, fixed mirror 26 and beam splitter 21. The interferometer utilizes a moving mirror 24 to produce constructive and destructive interference patterns at detector 25. These patterns depend upon the frequency or wave number of the detected light as well as the characteristics of the sample. Mirrors 26 and 27 direct the path of the light from the source to the sample. Circuitry (not shown) is provided for performing a Fourier transform of the return signal arriving at detector 25. (A person

skilled in the art is familiar with suitable circuitry for performing such a Fourier transform.)

[0014] In the case of arsenic as the dopant for creating the buried plate, it has been found according to the preferred embodiment that the portion of the spectrum between 400 and 1500 wave numbers shows a specific absorption band which is deemed to be attributed to a vibration of the As-O band. This absorption band is characterized by two absorption peaks, one around 1020 wave numbers and another between 700 and 800 wave numbers. The pattern of this absorption band and the ratio of the heights of these two peaks is changed significantly with increasing D_{BP} In fact, each D_{BP} depth causes a very distinct pattern in this portion of the spectrum which can be used as described herein for measuring the buried plate depth non-destructively by means of pattern comparison.

[0015] In particular, the spectral content of the return signal for several samples of known buried plate depth are analyzed to create a body or library of reference or calibration spectra. If desired, the library can include different sets of calibration spectra, for example, a set for each DRAM generation, such that in use, the device would be comparing the return signal only to the proper set of spectra that match the characteristics of the wafer being tested. The known buried plate depth of analyzed samples is determined by cross-section highlighted or contrast etching of the outdiffused area and scanning electron microscope (SEM) measurement. According to the preferred embodiment, the unknown sample is illuminated with the IR light and the spectral content of the return signal is analyzed to determine which of the reference or calibration spectra the unknown spectrum most closely matches. The reference spectrum which most closely matches the unknown spectrum indicates the depth of the top of the buried plate.

[0016] According to preferred aspects of the present invention, for maximizing the comparison, the calibration spectra is truncated at 440 cm⁻¹ and at 1180 cm⁻¹ and the intensity of the values is normalized between 0 and 1. Likewise, the spectra from the unknown sample whose D_{BP} needs to be determined is also truncated at 440 cm⁻¹ and at 1180 cm⁻¹ and intensity normalized to values between 0 and 1.

[0017] The process of finding the matching known spectrum can be performed by a least squares comparison of the unknown spectrum to some or all of the known spectra. For example, SUM i = 1 to i = n of corresponding points $(a_i - b_i)^2$ along each curve is used to find the minimum sum. In other words, the least square fit procedure involves calculating the difference for each wave number and each calibration spectrum; squaring the difference for each wave number and each calibration spectrum; summing up the squares for all wave numbers and each calibration spectrum; and determining the minimum of all sums. The minimum is found for the best fitting calibration spectrum and the $D_{\rm BP}$ of the sample is the same as the one of the calibration spec-

trum. Of course, other correlation methods can be used if desired such as by calculating the covariance "COV" or the Correlation Coefficient ρ_{xy} as described in Users' Guide Microsoft[®] Excel.

[0018] The Covariance tool returns the average of the product of deviations of data points from their respective means. Covariance is a measure of the relationship between two ranges of data.

$$cov(X,Y) = \frac{1}{n} \Sigma(x_1 - \mu_X)(y_1 - \mu_Y)$$

wherein μ_x is the mean value of x-data set and μ_y is the mean value of y-data set.

[0019] The Correlation tool measures the relationship between two data sets that are scaled to be independent of the unit of measure. The population correlation calculation returns the covariance of two data sets divided by the product of their standard deviations.

$$\rho_{X,y} = \frac{cov(X,Y)}{\sigma_X \cdot \sigma_y}$$

where σ_y is standard deviation of y-data set; where σ_x is standard deviation of x-data set; where

$$\sigma_x^2 = \frac{1}{n} \Sigma (X_I - \mu_x)^2$$

and

$$\sigma_y^2 = \frac{1}{n} \Sigma (Y_i - \mu_y)^2$$

[0020] Fig. 6 contains curves showing the spectral content of known and unknown samples having different buried plate depth measurements. Fig. 6 is the plot after being normalized in intensity and ready for comparison such as by the least squares method to the unknown sample which appears on the plot. The unknown sample in Fig. 6 fits most closely to the curve representing a depth of 1.53 μ m. Also, it should be understood that increasing the number of correlation curves increases the accuracy of the measurement.

[0021] Fig. 7 is a graph confirming by SEM cross-sectioning the depth measures obtained by FTIR. Values on the x-axis are from FTIR. Values on the y-axis are from SEM.

Claims

 A method for measuring the depth of a buried interface below the surface in a semiconductor substrate comprising: illuminating the semiconductor substrate containing the buried interface to be measured with infrared light;

detecting and analyzing the spectral content of a return signal by Fourier analysis; and comparing the spectral content of said return signal to calibration spectra to thereby determine the depth of said buried interface.

- The method of claim 1 wherein said infrared light is broadband IR radiation.
 - The method of claim 2 wherein the wavelength of said IR radiation is 2-25 microns.
 - 4. The method of claim 1, 2 or 3 wherein said buried interface is the top of a buried conductive plate.
- The method of claim 4 wherein the depth of the top
 of said buried conductive plate is about 1.5 ± 0.15
 microns below the surface of the semiconductor
 substrate.
 - The method of claim 4 or 5 wherein said buried conductive plate is arsenic.
 - The method of claim 6 wherein absorption bands at about 1020 wave numbers and between 700 and 800 wave numbers have absorption peaks.
 - The method of any preceding claim wherein said comparing employs a least squares comparison of the spectra from the sample compared to the calibration spectra.
 - The method of any preceding claim wherein the intensity of the values is normalized between 0 and 1 prior to the comparing.
 - 10. A device for determining the depth of a buried intertace below the surface of a semiconductor substrate, comprising:

an FTIR spectrophotometer which illuminates said substrate with a source of infrared radiation and which produces a Fourier transform of a return signal reflected from said substrate; a library of stored calibration spectra; and means for comparing said Fourier transform return signal to said calibration spectra to determine the depth of said buried interface.

- The device of claim 10 wherein said source of infrared light is a source of broadband IR radiation.
- 12. The device of claim 11 wherein the wavelength of said IR radiation is 2-25 microns.

4

25

30

35

BNSDOCID: <EP 0929094A2 1 >

13. The device of claim 10, 11 or 12 wherein said means for comparing comprises a least squares comparison means for comparing the spectra from said substrate to said calibration spectra.

14. The device of any of claims 10 to 13 which further comprises means for normalizing the intensity of said return signal between 0 and 1.

15. The device of any of claims 10 to 14 wherein said library of stored calibration spectra comprises stored calibration spectra for a buried conductive plate.

16. The device of claim 15 wherein said library of stored calibration spectra comprises calibration spectra for a buried arsenic containing conductive plate.

The device of any of claims 10 to 16 wherein said 20 library contains different sets of calibration spectra.

 The device of claim 17 wherein said different sets includes a set of calibration spectra for each DRAM generation.

30

35

40

45

50

FIG.1
PRIOR ART

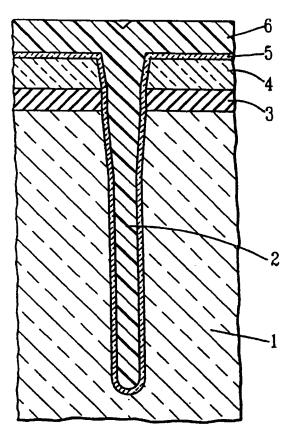


FIG. 2
PRIOR ART

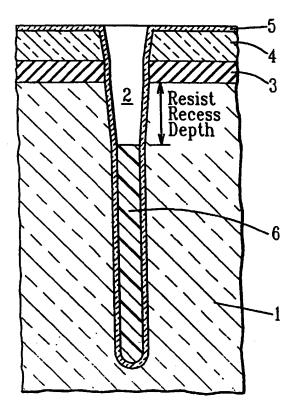


FIG. 3 PRIOR ART

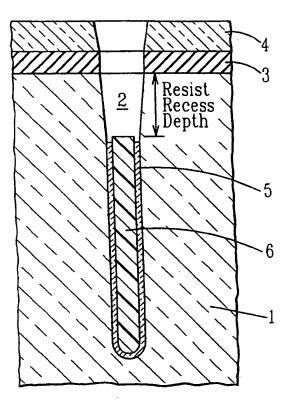


FIG. 4
PRIOR ART

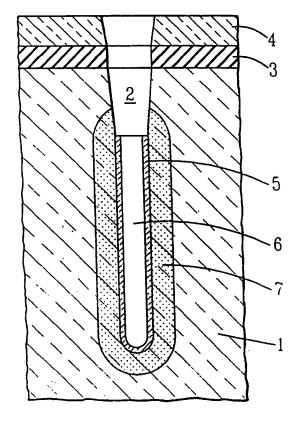
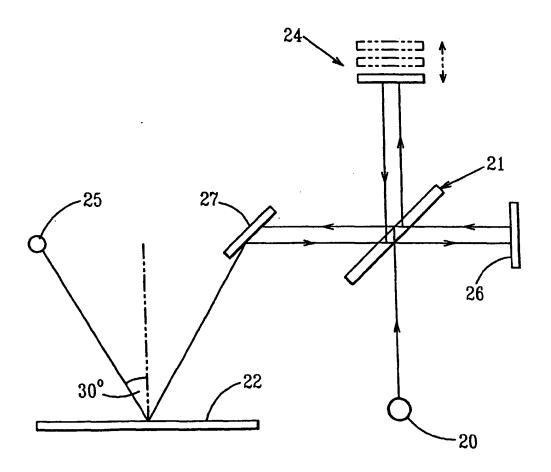


FIG. 5



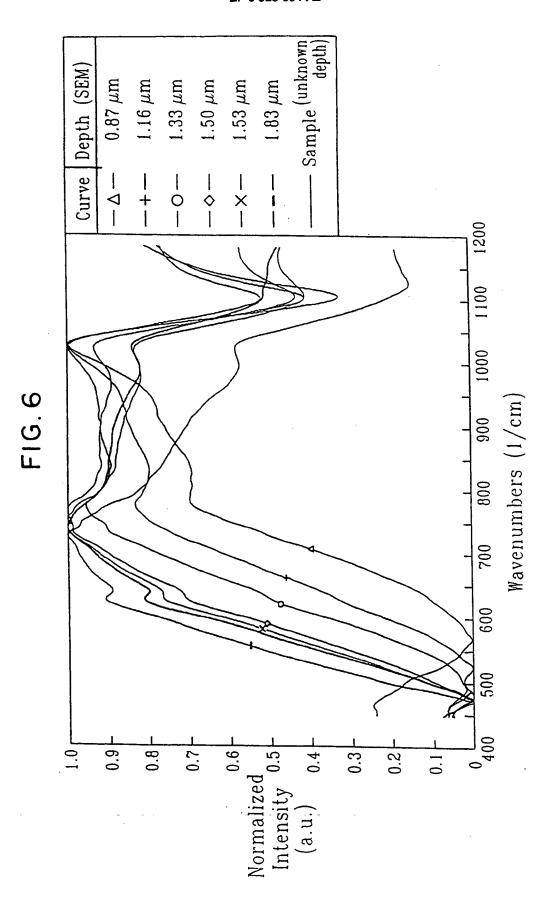
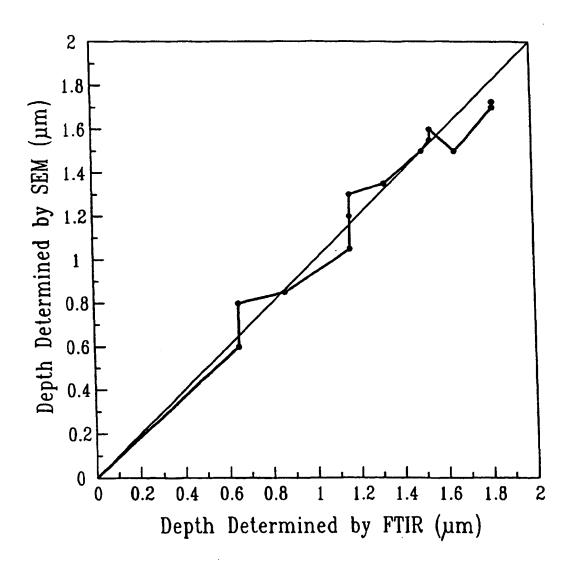


FIG. 7





Europäisches Patentamt

European Patent Office

Office européen des brevets



EP 0 929 094 A3

(12)

EUROPEAN PATENT APPLICATION

(88) Date of publication A3: 27.12.2000 Bulletin 2000/52

(43) Date of publication A2: 14.07,1999 Bulletin 1999/28

(21) Application number: 98310258.3

(22) Date of filing: 15.12.1998

(51) Int. Cl.⁷: **H01L 21/00**, G01R 31/265, G01R 31/26, G01N 21/55, G01B 11/06, H01L 21/66

(11)

(84) Designated Contracting States:

AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE Designated Extension States: AL LT LV MK RO SI

(30) Priority: 07.01.1998 US 4074

(71) Applicants:

 International Business Machines Corporation Armonk, NY 10504 (US)

• SIEMENS AKTIENGESELLSCHAFT 80333 München (DE)

(72) Inventors:

Muller, Paul K.
 Wappingers Fails, New York 12590 (US)

 Jaiprakash, Venkatachalam C. Beacon, New York 12508 (US)

(74) Representative:

Davies, Simon Robert
IBM,
United Kingdom Limited,
Intellectual Property Law,
Hursley Park
Winchester, Hampshire SO21 2JN (GB)

(54) Method and device for measuring the depth of a buried interface

(57) The invention discloses a method for measuring the depth at which a buried interface below the surface in a semiconductor substrate is located in a non-destructive manner which employs Fourier Transform Infrared (FTIR) measurements.

The method includes illuminating the semiconductor substrate containing the buried interface to be measured with infrared light and detecting and analyzing the spectral content of a return signal by Fourier analysis. It further involves comparing the spectral content of the return signal to calibration spectra to thereby determine the depth of the buried interface.

In addition a device is also provided for measuring the depth of a buried interface.

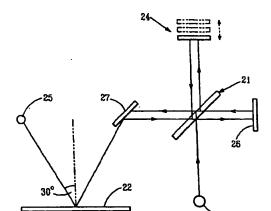


FIG. 5

Printed by Xerox (UK) Business Services 2.16.7 (HRS)/3.8



EUROPEAN SEARCH REPORT

Application Number

EP 98 31 0258

- 1	DOCUMENTS CONSIDE	RED TO BE RELEVANT	 	
ategory	Citation of document with income of relevant passa		Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.C1.6)
(US 5 229 304 A (CHAN 20 July 1993 (1993-C * the whole document	7-20)	1,2,10,	H01L21/00 G01R31/265 G01R31/26 G01N21/55
(24 December 1996 (19	HIZAWA SEIJI ET AL) 996-12-24) - column 2, line 61 *	1,10	G01B11/06 H01L21/66
4	EP 0 639 753 A (DAII 22 February 1995 (19 * claim 1 *		1,10	
Ą	US 4 555 767 A (CAS 26 November 1985 (1 * abstract *		1,10	
A	US 5 227 861 A (HAT 13 July 1993 (1993- * abstract *		1,2	TECHNICAL EIE DC
			-	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
				G01B H01L G01N G01R
	The present search report has	been drawn up for all claims		
	Place of search	Date of completion of the sear	ľ	Examiner
I	THE HAGUE	7 November 200	00 V:	ytlacilová, L
Y:p d A:te	CATEGORY OF CITED DOCUMENT: enticularly relevant if taken alone enticularly relevant if combined with an ecument of the same category achnological background non-written disclosure	E : earlier pale after the fill ther D : document c	cited in the applicat cited for other reaso	ublished on, or lian ons

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 98 31 0258

This arnex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

07-11-2000

Patent document cited in search repo		Publication date		Patent family member(s)	Publication date
US 5229304	Α	20-07-1993	NONE		· ·
US 5587792	A	24-12-1996	JP EP US	7004922 A 0631106 A 5523840 A	10-01-1999 28-12-1999 04-06-1999
EP 0639753	A	22-02-1995	JP JP DE DE US	2840181 B 7055435 A 69408608 D 69408608 T 5440141 A	24-12-199 03-03-199 02-04-199 03-09-199 08-08-199
US 4555767	Α	26-11-1985	NONE		
US 5227861	A	13-07-1993	JP JP DE DE DE EP	2728773 B 4120404 A 3110405 A 69021813 D 69021813 T 69033111 D 69033111 T 0420113 A 0650030 A	18-03-199 21-04-199 10-05-199 28-09-199 23-05-199 17-06-199 09-09-199 03-04-199
					·

For more details about this annex :see Official Journal of the European Patent Office, No. 12/82